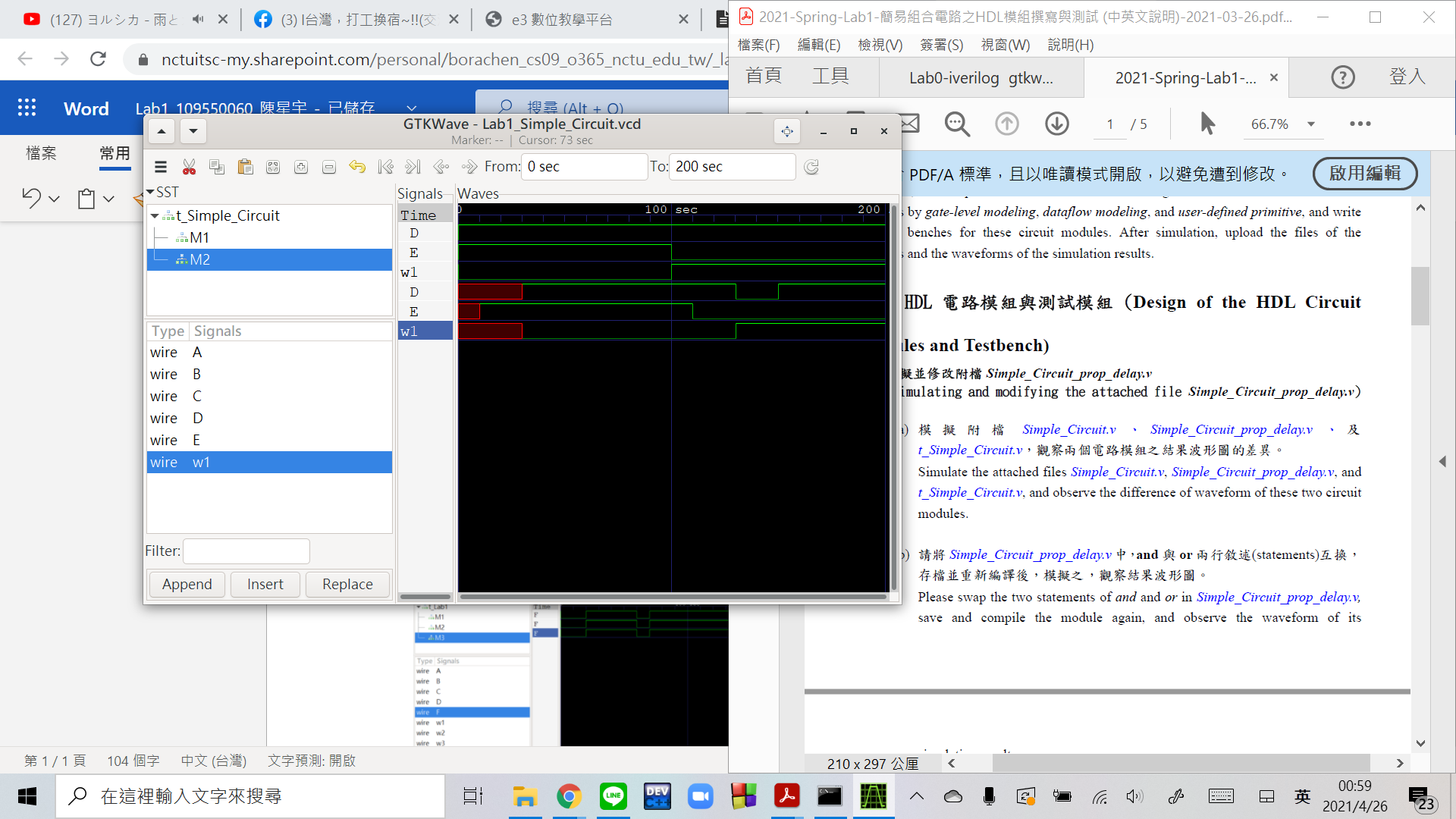
1.



Output E:

Simple\_Circuit\_prop\_delay(M2) has 10 time units delay compared with Simple\_Circuit(M1) as a result of NOT gate delay.

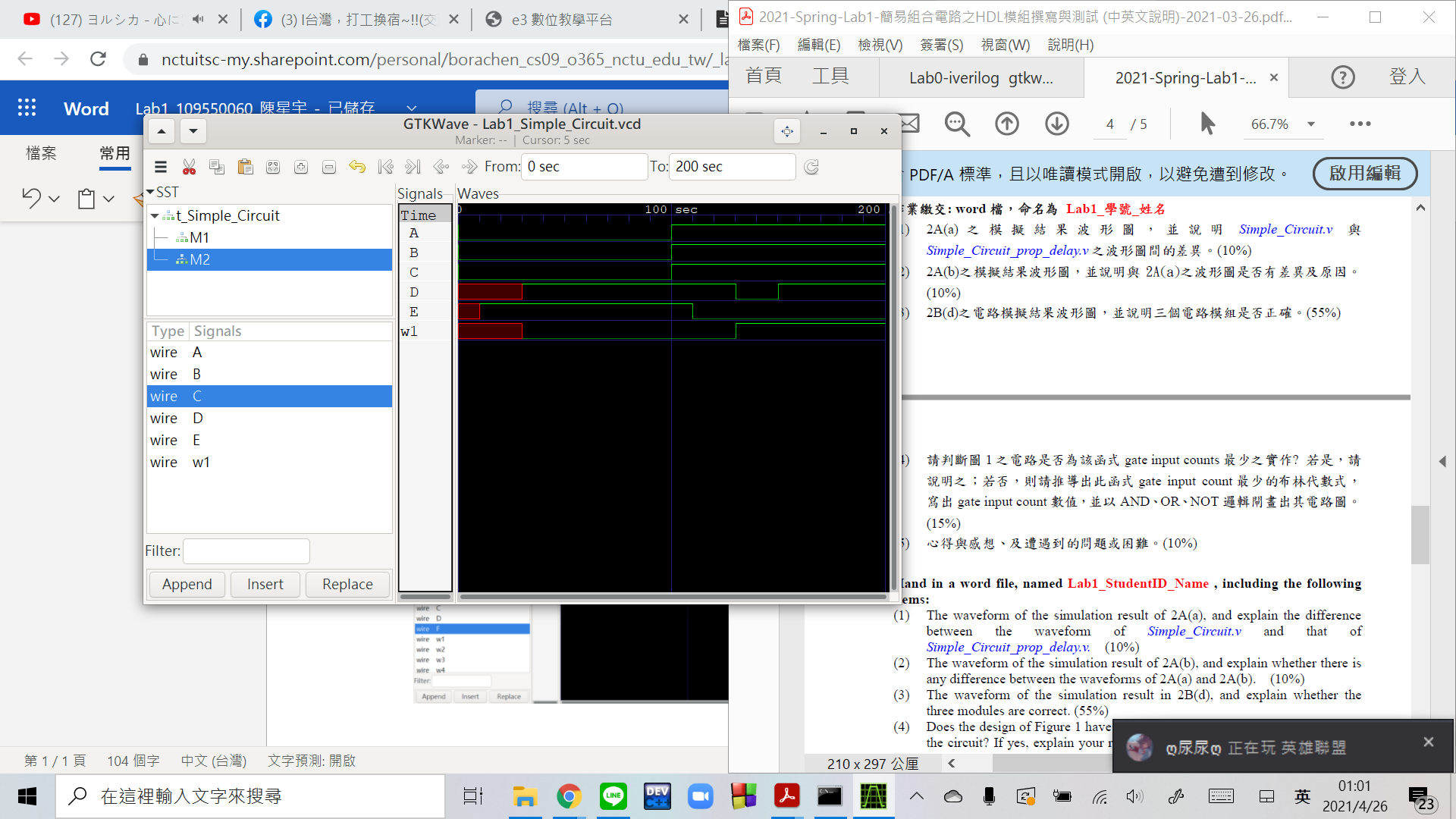
Wire w1:

M2 has 30 time units delay compared with M1 as a result of AND gate delay.

Output D:

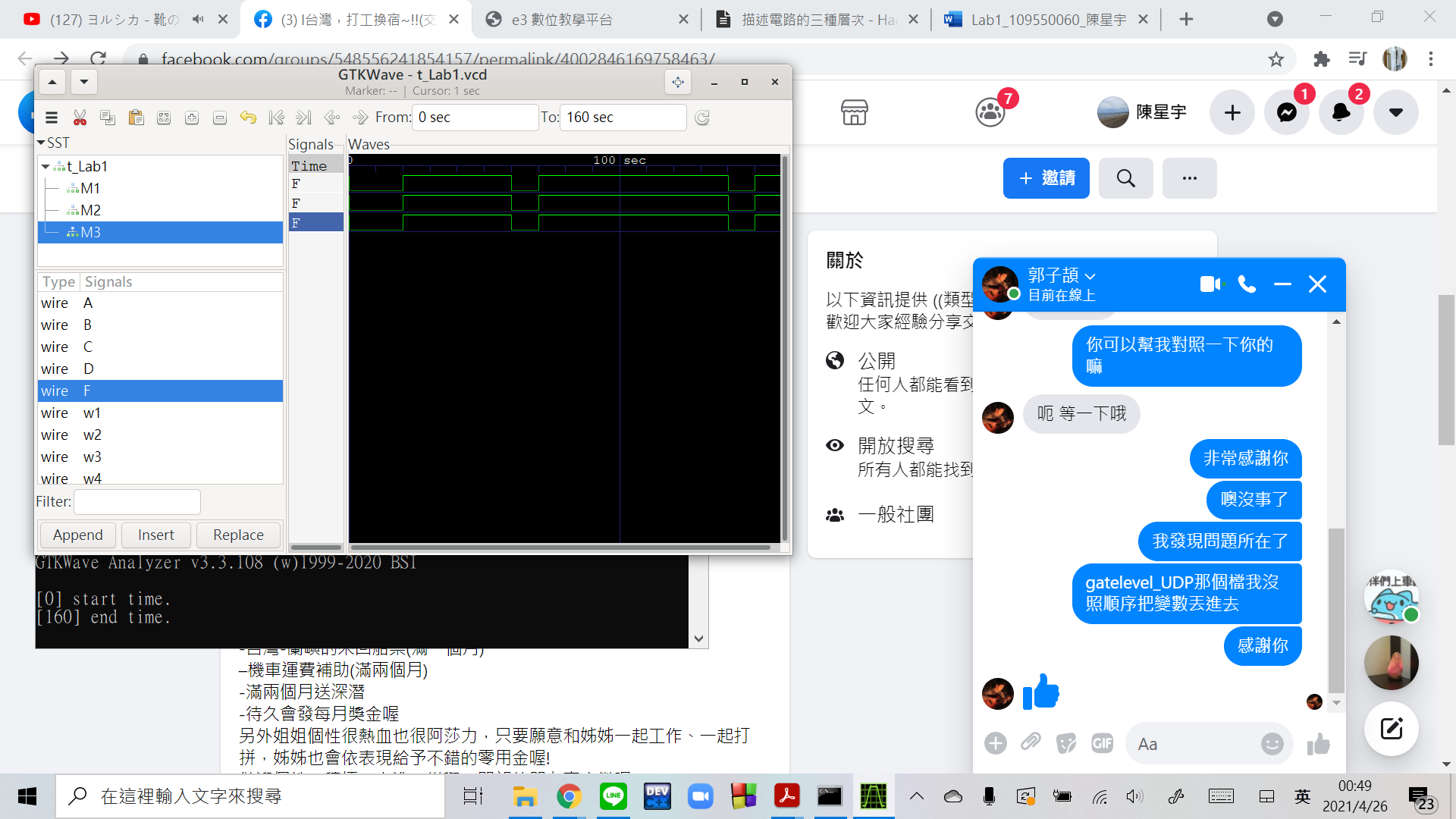
M2 has 20 time units delay on OR gate and combined with the E,w1 delay before,it is 0 at 130~150time units compared with M1.

2.



與 2A(a)之波型圖無異，原因為變動的只有gate的建立順序，最後建出的電路途仍與原本一樣。

3.



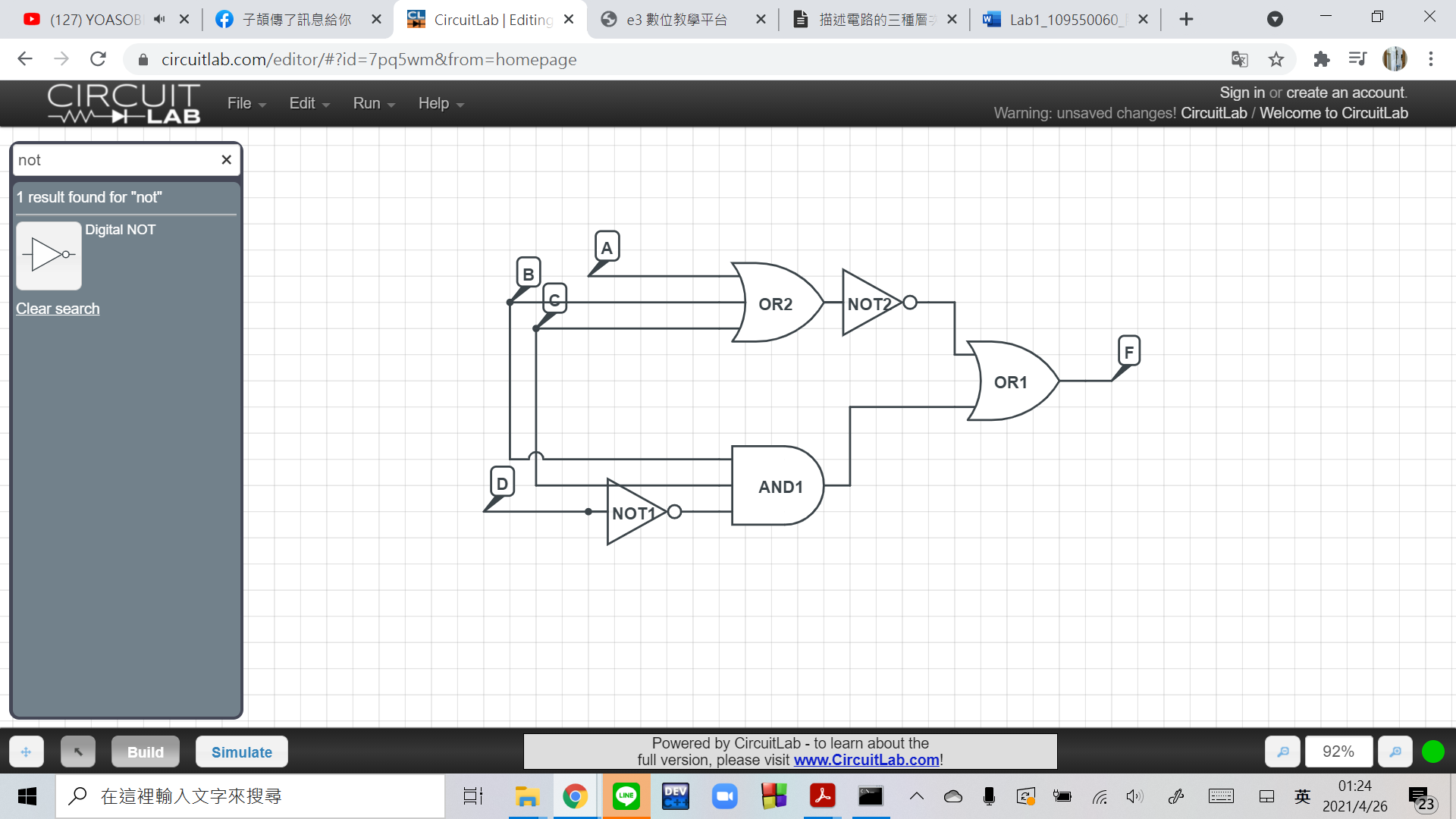
每10個time units 為一個不同的輸入，直到160個time units finish 前從m0依序輸入到m15，發現每個輸出F皆一樣，即三個電路模組等價。

4.

use K’map to simplify it to SoP

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 |  |  |
|  |  |  | 1 |
|  |  |  | 1 |
|  |  |  |  |

A'B'C' + BCD' = (A+B+C)' + BCD' GIC:10



5.

我一開始在做完testbench要run的時候發現我UDP那項的輸出和其他兩個不一樣，回去看程式才發現是因為那項的輸出和其他兩個不一樣，回去看程式才發現是因為gatelevel\_UDP的檔案輸入順序和UDP的不一樣，除此之外都沒什麼問題，也覺得可以親手實作電路還滿有趣的。